these claims, rewritten claims 2, 4, 15, 16, 23, 24, 58 & 59 are believed in condition for allowance pursuant to the first Office Action, while amended claims 1, 3, 5-14, 17-22, 56, 57, 60 & 61 are believed allowable for the reasons stated below.

Initially, claim 6 has been amended to address the indefiniteness rejection stated in the first Office Action. Specifically, the language "thermally or chemically removable" has been deleted from the claim, and applicant now recites that the release layer comprises one of a thermoplastic material or a solventable material. Support for this amendment can be found throughout the application. For example, reference page 30, lines 17-19 (wherein the "transition layer" comprises the release layer), and page 31, lines 8-11 where a solvent cleaning of the second dielectric (again the release layer) is discussed. In view of these amendments to claim 6, removal of the 35 U.S.C. §112, second paragraph, rejection is requested.

Substantively, original claims 1, 5, 13, 14, 17, 19, 20, 22 and 56-57 were rejected under 35 U.S.C. §102(b) as being anticipated by Fillion et al. (U.S. Pat. No. 5,315,486), while claims 8, 9, 10, 11, 18 & 21 were rejected under 35 U.S.C. §103(a) as being obvious over Fillion et al. Each of these rejections is respectfully, but most strenuously, traversed to any extent deemed applicable to the amended claims presented herewith.

As defined in amended independent claims 1, 19 & 56, applicant's invention comprises a multichip or single chip module structure wherein each chip in the module has structural material surrounding and physically contacting its at least one side surface. The structural material has an upper surface co-planar with the upper surface of each chip so that a co-planar front surface is defined, and a lower surface substantially parallel with the lower surface of each chip, thereby defining a back

surface of the module. Applicant respectfully submits that this structural material (as recited in the independent claims presented herewith) lends patentability to the multichip and single chip modules recited herein. The structural material is further qualified in new claims 60 & 61 which recite that no space is defined between the material and the at least one side surface of each chip of the module. Applicant respectfully submits that a structural material as recited herein which physically contacts the at least one side surface of each chip (and which leaves no spaces between the side surfaces of the chips and the material) is incapable of being obtained from the teachings, suggestions and implications of Fillion et al.

With respect to the anticipation rejection, it is well settled that there is no anticipation unless (1) all the same elements are (2) found in exactly the same situation and (3) are united in the same way to (4) perform the identical function. As amended, applicant's independent claims and the structures of Fillion et al. clearly do not have the same elements united in the same way to perform the identical function, and these differences provide significant advantages to applicant's structure.

The Fillion et al. patent is an example of a high density interconnect (HDI) approach such as depicted in Fig. 2 of the present application. In the HDI (or Fillion et al.) approach, instead of thinning chips to a predetermined thickness the substrate 32 (Fig. 2 of the present application) is machined with wells 34 of different depths (see also Fig. 2 of Fillion et al.). When the chips are placed in the substrate wells, the tops of the chips are disposed even with the top surface of the substrate. An adhesive is then applied to the tops of the chips and a pre-processed layer of polymer film is laminated above the chips. Via holes are formed in this overlay layer above the pads of the IC chips and metallization is sputtered on the surface of the

overlay layer and in the via holes. The metallization is subsequently built up electrolytically and patterned by photolithographic means. Additional interconnect layers are built up as required by depositing dielectric using coating or laminating means, forming via holes, and then metallizing and patterning.

Applicant respectfully submits that a careful reading of Fillion et al. fails to uncover any teaching of a structural material for a multichip or single chip module characterized as now recited. Having been aware of the Fillion et al. structure, applicant's original recitation of a structural material "surrounding" the at least one side surface was intended to recite the concept of "physically contacting" the at least one side surface. This is now expressly stated in the amended independent claims presented herewith. Support for "physically contacting" can be found throughout the present application, and in particular, in drawing FIGs. 4-9(e). Since Fillion et al. employs wells 20 to accommodate the chips 22, there must be space between the chips and the inner surface of each well to allow the chip to be placed within the well. Fillion et al. describes forming the wells or cavities using laser or machining technology and then placing the chips into these wells. As a practical matter, there must be sufficient room to place a chip into its corresponding well. This is contrasted with the present invention wherein the structural material surrounds and physically contacts the at least one side surface of each chip in the module.

The above-noted difference to applicant's invention and the teachings of Fillion et al. is significant. With a structure such as Fillion, there necessarily is a gap or space between the side surfaces of the chips and the side wall defining the well within which the chip is placed. Because of this gap, Fillion et al. is unable to directly apply liquid dielectric material to the

top planar surface of the substrate/chip assembly. Thus, Fillion et al. expressly teach that the first surface 28 comprises a pre-processed (cured) material. This pre-processed material covers the gaps formed between the inner walls of the wells and the side surfaces of the chips within the wells.

With respect to claim 1, applicant also recites that an in situ process layer is disposed directly on the front surface. As described in the present application, this in situ process layer is a photo-patternable layer (claim 17). This structure is also significant. During fabrication, applicant's structure has the advantage of allowing the first layer dielectric to be sprayed on and then be photo-processed. In the Fillion et al. structure, the pre-processed layer applied to the top surface of the substrate and chips must be laser processed.

As a practical matter, applicant respectfully submits that there is no suggestion in the art for modifying the structure of the Fillion et al. patent to somehow have the substrate material surround and physically contact the at least one side surface of each chip. To subsequently fill the well gaps in Fillion et al. would be very difficult. If the process overfilled, then bumps would exist on the upper surface of the assembly, while underfilling wouldn't achieve the desired objective. Applicant's novel structure is obtained by a novel processing method as described in the present application.

Since the above-noted structural features of applicant's module, and the function thereof, are absent from the Fillion et al. patent, applicant respectfully submits that independent claims 1, 19 & 56 would not have been anticipated by, or even obvious to one of ordinary skill in the art, in view of Fillion et al. Thus, reconsideration and removal of the anticipation rejection thereof is respectfully requested. Dependent claims 5, 13, 14, 17, 20, 22 & 57 are believed allowable for the same

reasons as the respective independent claim from which they depend, as well as for their own additional characterizations.

For example, claims 17 & 20 recite that the in situ process layer on the front surface of the module comprises a photo-patternable dielectric material. This structure is different from that described in Fillion et al. As noted, the first layer on the substrate/chip assembly in Fillion et al. comprises a pre-processed layer. This pre-processed layer is a cured polyimide and since the polyimide is cured, it is no longer photo-patternable. Thus, applicant respectfully traverses the Examiner's characterization of Fillion et al. with respect to claims 17 & 20. Fillion et al. would require photo-ablation (laser light) in order to pattern the pre-processed polyimide. In contrast, applicant recites that the in situ process layer is a photo-patternable layer, which would be understood by one skilled in the art to mean patternable using conventional masking and UV exposing techniques. Reference page 9, line 25 of the present application wherein laser-ablation is specifically excluded from the definition of photo-patterning as employed by applicant (and as employed by those skilled in the art).

Regarding the remaining claims, applicant respectfully requests reconsideration and withdrawal of the obviousness rejection (to claims 8, 9, 10, 11, 18 & 21) for the reasons stated above in connection with the anticipation rejection to the independent claims. An "obviousness" determination requires an evaluation of whether the prior art taken as a whole would suggest the claimed invention taken as a whole to one of ordinary skill in the art. Even if all the elements of a claim are disclosed in various prior art references, the claimed invention taken as a whole cannot be said to be obvious without some reason given in the prior art why one of ordinary skill in the art would have been prompted to combine the teachings of the references to arrive at the claimed invention. In evaluating claimed subject

matter as a whole, the Federal Circuit has expressly mandated that functional claim language be considered in evaluating a claim relative to the prior art. Applicant respectfully submits that the application of these standards to independent claims 1, 19 & 56 leads to the conclusion that the recited subject matter would not have been obvious to one of ordinary skill in the art based upon the teachings of Fillion et al.

In analyzing the independent claims "as a whole" there exist limitations in the claims which are simply not taught, suggested or implied by Fillion et al. Specifically, each independent claim presented herewith recites that there is a structural material "surrounding and physically contacting the at least one side surface of each chip." Again, the Fillion et al. technique is to create wells within the substrate using laser ablation or machining which are sized to accommodate chips so that an upper planar surface of each chip is co-planar with an upper surface of the substrate. In order to place the chips within the wells, space must exist between the side surface of the chip and the inner surface of the well. The space is specifically shown in the drawings of Fillion et al. Based upon this process teaching, applicant respectfully submits that there is no suggestion in Fillion et al. to make the process modifications which would be necessary to achieve applicant's recited structure. Since there is no basis for modifying the reference, applicant respectfully submits that the independent claims would not have been obvious to one of ordinary skill in the art based upon Fillion et al. The dependent claims are believed allowable for the same reasons as the independent claims as well as for their own additional characterizations.

No new matter is added to the application by any amendment presented herewith. In view of the above amendments and remarks, applicant respectfully requests allowance of all claims pending herein. If, however, the Examiner believes any issue remains

unresolved, the Examiner is requested to telephone applicant's undersigned representative to further discuss the case.

Respectfully submitted,

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Dated: May 07, 1998

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